

Features

- OIF-compliant SPI-4 Phase 2 (compatible with Saturn Group POS-PHY L4)
- Fully synchronous design, exceeds: 1 Gb/s (500 MHz DDR)
- 16-bit external data bus width. 64- or 128-bit internal data bus width
- Single- and multi-channel operation, scalable from 1 to 256 channels.
- Multi-channel FIFOs with programmable size
- PluriBus™ User Interface for seamless integration with other Modelware cores for bridge and mux/demux designs
- Out-of-band packet signaling with SOP, EOP, Mod, and Err on PluriBus User Interface.
- SOP/EOP checking
- Normal and high-speed FIFO Status Channel (run-time selectable)
- Automatic sink flow control generation (RStat)
- Source flow control processing (TStat), per channel credit management, and source data scheduler
- Packet segmentation and reassembly
- Hitless Bandwidth Provisioning
- Start Of Packet (SOP) data to MSB alignment function.
- Handles continuous back-to-back End Of Packets (EOP) ($2^N + 1$ -byte packets) with shared control words¹
- DIP-4/DIP-2 Parity generation/checking¹
- Advanced protocol error checking
- Training Sequence generation and detection
- Static alignment with programmable clock/data relationship
- Dynamic alignment capable of compensating for skew and jitter of up to 3 bit times (pk to pk) with a single training pattern.
- ASIC and FPGA support
- Fully automatic test bench including sophisticated SPI-4.2 driver/monitor.

Standards Compliance

- OIF SPI-4 Phase 2
- Saturn Group (PMC-Sierra) POS-PHY L4
- Verified standard compliance using PMC-Sierra's POS-PHY L4 models.

Description

The Optical Interworking Forum's (OIF) SPI-4 Phase 2 interface allows the interconnection of Physical Layer devices to Link Layer devices in 10Gb/s ATM, POS, and Ethernet applications. Modelware's SPI-4.2 Manager core is a full implementation of the SPI-4.2 specification including per-channel packet buffering. Figure 1 shows a typical application of the SPI-4.2 Manager core.

On the user's side, the SPI-4 Phase 2 Manager core interfaces to multiple channels through multi-channel FIFOs. The core completely handles the FIFO status channel with no user interaction. The SPI-4 Sink section transmits the FIFO status information for each channel according to the fill level of the Sink multi-channel FIFO and reassembles packets received for a particular channel in that channel's FIFO. The SPI-4 Source section receives the far-end FIFO status from the FIFO Status Channel and uses the flow control information in the Credit Manager for scheduling. The Source section transmits data segments to a particular channel from that channel's FIFO.

¹ Patent Pending Technology

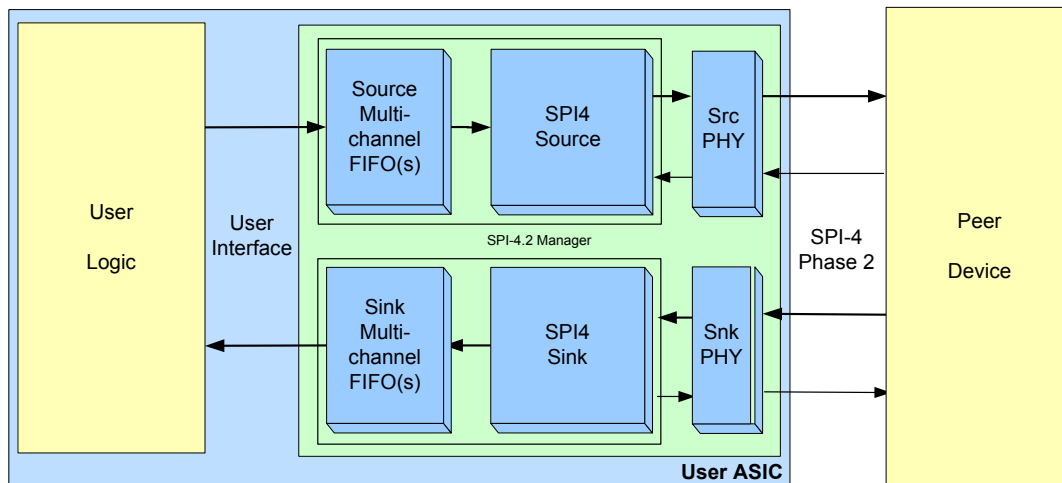


Figure 1: SPI-4 Phase 2 Manager Application

Design Package

The SPI-4.2 Core source code package contains:

- Source code or Netlist
- System test bench (source code option)
- Scripts and data files for simulation, ASIC and FPGA synthesis, and FPGA layout
- Detailed documentation

ASIC Technology

The SPI-4.2 Core, including the PHY Layer is a synthesizable soft core and is compatible with any ASIC technology. The core has been successfully implemented in the following technologies:

- IBM: 0.13
- KLSI: 0.13
- LSI: 0.18 and 0.13
- NEC: 0.13
- TI: 0.13
- TSMC: 0.18, 0.15, and 0.13
- UMC: 0.13

Interoperability

The SPI-4.2 Core has successfully interoperated with devices from the following ASSP manufacturers:

- AMCC
- Dune Networks
- Intel
- Network Elements
- PMC-Sierra
- Zettacom/IDT

Supported Tools

- Synthesis:
 - Mentor Graphics – Precision Synthesis
 - Synopsys – Design Compiler
- FPGA Layout:
 - Altera – Quartus II
 - Xilinx – ISE

Ordering Information

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