

### Features

- OIF-compliant SPI-4 Phase 2 (compatible with Saturn Group POS-PHY L4)
- Fully synchronous design, exceeds: 1 Gb/s (500 MHz DDR)
- 16-bit external data bus width. 64-bit internal data bus width
- Single- and multi-link operation, scalable from 1 to 256 links.
- Single Sink and Source FIFOs for all channels
- Programmable FIFO size.
- PluriBus™ User Interface for seamless integration with other Modelware cores for bridge and mux/demux designs
- Normal and high-speed FIFO Status Channel (run-time selectable)
- Hitless Bandwidth Provisioning
- Start Of Packet (SOP) data to MSB alignment function.
- Handles continuous back-to-back End Of Packets (EOP) ( $2^N + 1$ -byte packets) with shared control words<sup>1</sup>
- DIP-4 Parity generation/checking<sup>1</sup>
- Advanced protocol error checking
- Training Sequence generation and detection
- Static alignment with programmable clock/data relationship
- Dynamic alignment capable of compensating for skew and jitter of up to 3 bit times (pk to pk) with a single training pattern.

- ASIC and FPGA support
- Fully automatic test bench including sophisticated SPI-4 Phase 2 driver/monitor.

### Standards Compliance

- OIF SPI-4 Phase 2
- Saturn Group (PMC-Sierra) POS-PHY L4
- Verified functionality and standards compliance using PMC-Sierra's POS-PHY L4 models.

### Description

The Optical Interworking Forum's (OIF) SPI-4 Phase 2 interface allows the inter-connection of Physical Layer devices to Link Layer devices in 10Gb/s ATM, POS, and Ethernet applications. Modelware's SPI-4.2 Foundation core is a full implementation of the SPI-4.2 specification. shows a typical application of the SPI-4.2 Foundation core.

On the user's side, the SPI-4 Phase 2 core interfaces to applications with a single or multiple channels through a single FIFO. The core passes the per-channel user FIFO status between the SPI-4 interface and the user's application. The SPI-4 Sink section transmits the FIFO status information provided by the user's circuitry. The SPI-4 Source section receives the far-end FIFO status from the FIFO Status Channel and makes it available for reading by the user's application. The SPI-4 Sink section stores data received for a particular channel in a single FIFO along with the channel address information that is decoded from the Control Word preceding the data burst.

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<sup>1</sup> Patent Pending Technology

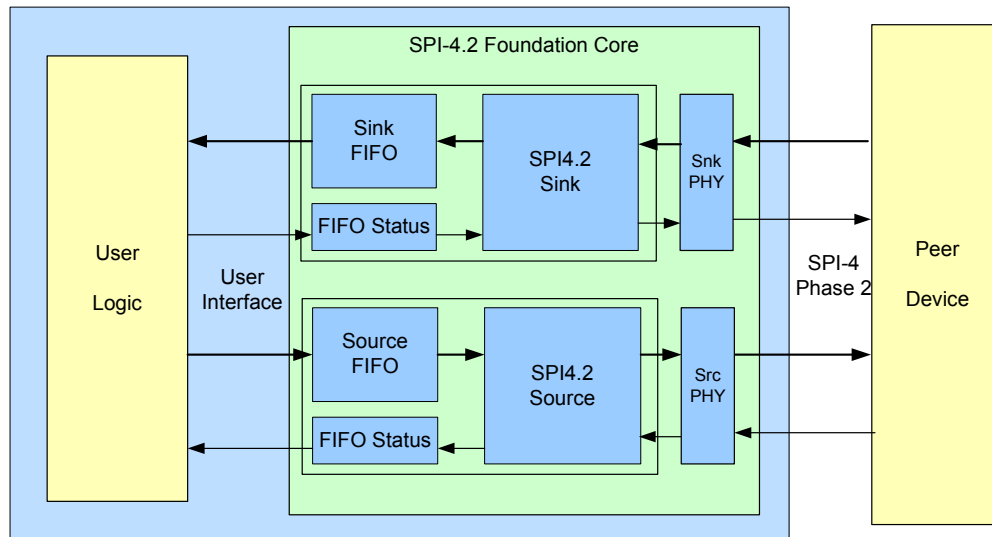


Figure 1: SPI-4 Phase 2 Foundation Application

## Design Package

The SPI-4 Phase 2 Core source code package contains:

- Source code or Netlist
- System test bench (source code option)
- Scripts and data files for simulation, ASIC and FPGA synthesis, and FPGA layout
- Detailed documentation

## ASIC Technology

The SPI-4.2 Core, including the PHY Layer is a synthesizable soft core and is compatible with any ASIC technology. The core has been successfully implemented in the following technologies:

- IBM: 0.13
- KLSI: 0.13
- LSI: 0.18 and 0.13
- NEC: 0.13
- TI: 0.13
- TSMC: 0.18, 0.15, and 0.13
- UMC: 0.13

## Interoperability

The SPI-4.2 Core has successfully interoperated with devices from the following ASSP manufacturers:

- AMCC
- Dune Networks
- Intel
- Network Elements
- PMC-Sierra
- Zettacom/IDT

## Supported Tools

- Synthesis:
  - Mentor Graphics – Precision Synthesis
  - Synopsys – Design Compiler
- FPGA Layout:
  - Altera – Quartus II
  - Xilinx – ISE

## Ordering Information

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